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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/686,243	10/14/2003	Vikram Kowshik	ATM-279	7611

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EXAMINER	
THAI, TUAN V	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/686,243	KOWSHIK ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14 and 15* is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/14/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Response to Amendment

1. This office action is in response to Applicant's communication filed January 03, 2006. This amendment has been entered and carefully considered. Claims 1-15 remain pending in the application. Claims 14-15 are allowed.

2. Applicant's arguments with respect to claims 21-29 and 31-46 have been fully considered but they are not deemed to be persuasive.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 11 are rejected under 35 U.S.C. § 102(b) as being anticipated by Kozaru et al. (USPN: 5,991,223); hereinafter Kozaru.

As per claim 1; Kozaru teaches the invention as claimed including a method of synchronous reading for a plurality of words in a memory system (e.g. see abstract; column 9, lines 38 et seq.) comprises selecting said plurality of words to be read (e.g. see column 13, lines 64-65), the plurality of words having a first group of words and at least one subsequent group of words; for example, memory array 1 contains multiple group of sub-arrays MA#0-MA#3 having multiple group of words (e.g. see column 13, lines 32 et seq.); reading said plurality of words into a plurality of data registers during a clock latency period (e.g. see column 14, lines 21 et seq.); and shifting out said plurality of words synchronously at the end of said latency period (e.g. see column 61-65).

As per claim 11, Kozaru discloses a burst mode operation system for fast synchronous reading in a memory system (e.g. see abstract) comprises a burst controller is taught a control circuit 902 for controlling burst operation adapted to receive an input clock signal, a variable latency signal, and a burst sequence control signal from said memory system to produce a plurality of words to be read and an output clock signal (e.g. see figure 27, column 1, lines 32 et seq.); an address controller is taught as read/write address circuit 910 coupled to said burst controller for producing addresses of said plurality of words to be read (e.g. see column 2, lines 6 et seq.); a two-tier column

decoder is taught as column decoder 908c (e.g. see figure 29) adapted to receive said addresses from said address controller for producing a first tier address and a second tier address (e.g. see column 3, lines 53 et seq.); and a row decoder is taught as global row decoder 908b (e.g. see figure 29) adapted to receive said addresses from said address controller for producing row addresses of said plurality of words to be read (e.g. see column 3, lines 50 et seq.).

Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozaru et al. (USPN: 5,991,223); hereinafter Kozaru, in view of Khang et al. (USPN: 6,111,808), hereinafter Khang.

As per claims 5 and 8, Kozaru discloses a two-tier column decoder to facilitate synchronous reading of a plurality of words in a synchronous memory system 1 (e.g. see figure 5;

column 3, lines 46 et seq.) comprises a sub bitline decoder is equivalently taught as global row decoder 5a coupled to a main bit line of said memory system for decoding row address signal from the address register (e.g. see figure 5; column 13, lines 38 et seq.); a first tier decoder is equivalently taught as decoder 5b coupled to global row decoder 5a to select both said even and odd addresses of said plurality of words for a first reading during a clock latency period (e.g. see figure 5; column 13, lines 40 et seq., lines 65 bridging column 4, line 9); and a second tier decoder is taught as block decoder 4 coupled to first tier decoder 5b to select either said lower or higher word addresses for a subsequent reading (e.g. see figure 5; column 14, lines 28 et seq.). Kozaru discloses the invention as claimed; Kozaru however does not particularly teach the global row decoder 5a for decoding a most significant bit of said plurality of words to be read and for determining whether an address of said plurality of words is in an low or high order word. Khang discloses the missing element that is known to be required in the system of Kozaru in order to arrive at the Applicant's current invention wherein Khang discloses the row decoder for decoding the a sub word line enable selection signal (SWLE) and a global word line signal (GWLb) utilized the most significant bit (MSB) and least significant bit address (LSB) scheme for determining locations of the address data/word (e.g.

see abstract; column 4, lines 55 et seq.). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention as made to employ the teaching of Khang wherein MSB and LSB addressing decoding scheme is utilized for determine address data/word location for that of Kozaru system. In doing so, first of all, it would allow location of the word address to be quickly recognized thru the implementation of least and most significant bit address; secondly, the system throughput would be greatly enhanced since decoding the MSB would take less number of system clock cycles, therefore being advantageous.

As per claim 8, see arguments with respect to claim 5. It encompasses the same scope of invention as to that of claim 5, the claim is therefore rejected for the same reasons as being set forth above.

Allowable subject matter

7. Claims 14-15 are allowed.

8. Claims 2, 6, 9, 12 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and intervening claims. Claims 3-4, 7 and 10 are also allowable since it is depended upon the indicated allowable claims 2, 6 and 9 respectively.

9. As per remark, Applicant's counsel asserts that (a) Kozaru fails to teach Applicant's claimed element of "selecting said plurality of words to be read, each of said selected plurality of words having a first group of words and at least one subsequent group of words; and reading selected plurality of words into a plurality of data registers during a latency period." (amendment, pages 9, last paragraph bridging page 10); (b) Kozaru fails to teach a burst controller adapted to receive a variable latency signal (amendment's page 10, last paragraph bridging page 11, fist paragraph); (c) Kozaru and Khang fail to teach the claimed invention (e.g. a sub bitline decoder, a first tier decoder ...(amendment, page 11 bridging second paragraph, page 13).

With respect to (a); Examiner would like to emphasize that Kozaru clearly discloses "selecting said plurality of words to be read, each of said selected plurality of words having a first group of words and at least one subsequent group of words; and reading selected plurality of words into a plurality of data registers during a latency period."; for example, starting at column 7, lines 31 et seq.; Kozaru discloses "in the operation of reading data from the memory cell, the local word line is selected, and then data of the selected memory cell is read onto the selected bit line pair and is subsequently transferred onto the local data bus line through the bit line peripheral circuit. Thereafter, the local sense amplifier is activated. In the data

write operation, the write driver drives the local data bus line pair to the potential level depending on the write data, and the write data is transmitted onto the bit line pair through the bit line peripheral circuit and is written into the memory cell."; (also see column 13, lines 64 et seq.). With respect to (b), first of all, Kozaru specifically disclose a burst controller as being equivalent to control circuit 902; it is this same controller that controlling burst operation mode of the static semiconductor memory (e.g. see column 1, lines 10 et seq.; figure 27); in addition, see column 17, lines 32 et seq.); Kozaru further discloses in the linear burst mode which is known to be controlled by the control circuit 902 (FIG. 19), block select signals BS0, BS1, BS2 and BS3 are cyclically activated in this order during the operation in the linear burst mode (column 24, lines 10 et seq.). The variable latency signal adapted to receive an input clock signal, a variable latency signal, and a burst sequence control signal from said memory system to produce a plurality of words to be read and an output clock signal (e.g. see figure 27, column 1, lines 32 et seq.); noting that the signals as indicated in figure 27 associated with the control circuit and as acknowledged by Applicant's counsel as clock signal ("CKL"), advance signal ("ADV"), address strobe signal ("ADS"), output enable signal ("OE"), and write enable signal ("WE") are known as variable latency signal, since variable

latency signal is the type of signal having different time required for output desired piece of data once processing is complete; these type of signals having different time requirement that clearly read on the claimed "variable latency" signal as contended by Applicant's counsel. With respect to (c), first of all the sub bitline decoder and a first tier decoder are taught by Kozaru as global row decoder 5a coupled to the main bit line and decoder 5b coupled to global row decoder 5a (e.g. see figure 5, column 13, lines 40 et seq.; lines 65 bridging column 4, line 9); secondly, in considering a 35 USC 103 rejection, it is not strictly necessary that a reference or references explicitly suggest the claimed invention (this is tantamount to a 35 USC 102 reference if the modifications would have been obvious to those of ordinary skill in the art. It has been held that the test of obviousness is not whether the features of a secondary reference may be bodily incorporated into the primary references' structure, nor whether the claimed invention is expressly suggested in any one or all of the references; rather, the test is what the combined teachings of the reference would have suggested to those of ordinary skill in the art. See In re Keller et al., 208 U.S.P.Q 871. In addition, Examiner further recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed

combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971). Korazu and Khang references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA) 1969. In this case, the Khang reference was used to provide evidence of global row decoder 5a for decoding a most significant bit of the plurality of words to be read and for determining whether an address of the plurality of words is in an low or high order word, Khang discloses the row decoder for decoding the a sub word line enable selection signal (SWLE) and a global word line signal (GWLb) utilized the most significant bit (MSB) and least significant bit address (LSB) scheme for determining locations of the address data/word (e.g. see abstract; column 4, lines 55 et seq.). The combination would allow location of the word address to be quickly recognized thru the implementation of least and most significant bit address; enhancing system throughput since decoding the MSB would take less number of system clock cycles, therefore being advantageous. The 35 USC §

103 rejection based on the combination of Hansen and Dowling is therefore deemed to be proper.

10. Applicant's arguments filed January 03, 2006 have been fully considered but they are not deemed to be persuasive.

11. **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be

obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see ***http://pair-direct.uspto.gov***. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/March 14, 2006

Tuan V. Thai
PRIMARY EXAMINER
Group 2100